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09/641,352	08/18/2000	Hidekazu Nagasawa	50090-237	5215

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EXAMINER
TON, DAVID

ART UNIT	PAPER NUMBER
2133	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

PPQ

Office Action Summary	Application No. 09/641,352	Applicant(s) Nagasawa et al.
	Examiner D. Tran	Group Art Unit 2133

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-13 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 1-13 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☑ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been ☑ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☑ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

1. Claims 1-13 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by **Tanaka** patent no. **5,550,987**.

As per claims 1 and 3:

Tanaka teaches the invention as claimed, including a data storage apparatus [see Fig. 2] comprising a crambling circuit [data transfer device 1 of Fig. 2] for converting an input signal [from input circuit 11 of Fig. 2] to a desired format [endian format, see claim 1], and a storage device [memory 6 of Fig. 2] for storing converted data;

wherein said scrambling circuit includes:

a plurality of conversion circuits [byte swap circuit 13 and word swap circuit 14 of Fig. 2] each converting said input signal according to different rules [see claim 28]; and

a selector [select circuit 12 of Fig. 2] for selecting one of signal output by said plurality of conversion circuits [see claim 28] and supplying what is selected to said storage device [see claims 15-20].

As per claim 2:

Tanaka teaches the invention as claimed, including a data storage apparatus [Fig. 2] comprising a scrambling circuit [data transfer device 1 of Fig. 2] for converting an input signal to a desired format [see claim 28], and a storage device [memory 6 of Fig. 2, see claim 15-20] for storing converted data;

wherein said scrambling circuit is constituted by a rewritable device [col. 1 lines 5-11].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Tanaka** patent no. **5,550,987**.

As per claims 4-6:

Tanaka teaches the apparatus includes a digital signal processor [CPU 4 of Fig. 2].

Tanaka does not teach the CPU for processing an output signal of an AD converter.

Official Notice is taken that an analog to digital converter circuit is well known.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply the CPU taught by Tanaka for processing any signal such as an output signal of an AD converter. This modification would have been obvious and a person having ordinary skill in the art

would have been motivated to do so because it would enhance the application of Tanaka invention for processing analog signal.

As per claims 7-9:

Tanaka teaches the apparatus includes an automatic address generation circuit [address counter 25 of Fig. 2] for generating address in response to commands from CPU 4 [see col. 10 lines 17-23].

Official Notice is taken that controlling internal process by external commands is well known.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the commands from CPU 4 as taught by Tanaka for external commands. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the external controllability of Tanaka invention.

As per claims 10-12:

Tanaka does not teach the apparatus includes a compression circuit for compressing data.

Official Notice is taken that a compression circuit for compressing data into a desired format is well known.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Tanaka to include a compression circuit for compressing data retrieved from storage for compressing data into a desired format. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the storage capability of Tanaka storage device.

6. Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over **Tanaka** patent no. **5,550,987** in view of **Tabata et al.** (Tabata) patent no. **6,154,862**.

As per claim 13:

Tanaka teaches a data storage apparatus according to claim 1 above; however, he does not teach a tester for testing a semiconductor device and for supplying said scrambling circuit with results of the testing.

Tabata teaches a tester [memory tester, title] for testing a memory and for supplying a failure analysis memory with results of the testing [see claim 1].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Tanaka for storing the results of testing of a semiconductor device generating from a tester as taught by Tabata. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the application of Tanaka device.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 746-7239 (Official)

(703) 746-7240 (Non-Official)

(703) 746-7238 (After-Final)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Davidton

dt

June 12, 2003

DAVIDTON
PRIMARY EXAMINER